48-59), first level and second level (column 3, lines 38-57)." The Applicant respectfully traverses the Examiner's rejection.

Nakatani et al. teach the use of two discrete and non-varying voltage levels, V_{CC} and V_{DR}, (column 3, lines 13-18). Nothing in Nakatani et al. either teaches or implies that either V_{CC} or V_{DR} are anything but static, invariant voltages. The claimed invention, however, discloses dynamically variable voltage levels which vary continuously during transition periods. As stated on page 6, lines 9-11, of the Specification "[d]uring transitional periods from non-activity to activity, the voltage is ramped up and then ramped back down." Claim 1 and Claim 23, as amended, teach "power control means. . . for supplying a variable voltage to said memory integrated circuit" (emphasis added), where

> said power being supplied to the memory integrated circuit at a first variable voltage level during periods of no data access activity and at a second variable voltage level during periods of data access activity, the variable voltage supplied at said first variable voltage level being less than the variable voltage supplied at said second variable voltage level

(emphasis added). Support for the amendment is found on, page 3 , line 17; Figure 2; and page 14, lines 1-3 and 14-16.

This claimed structure is neither anticipated nor suggested by Nakatani et al. The passage cited by the Examiner in support of Nakatani et al. disclosing "a variable voltage level" teaches switching between two fixed voltage levels. Claims 1 and 23, on the other hand, disclose supplying two different variable voltage levels. Therefore, Nakatani et al. teach away from the invention of Claims 1 and 23.

Accordingly, the Applicant respectfully submits that Nakatani neither anticipates nor suggests the invention of Claims 1-23 and respectfully requests withdrawal of the Examiner's rejection.

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The Examiner further rejected Claims 1-23 under 35 U.S.C. § 102(e), as being anticipated by Fung (US Pat. No. 5,396,635). The Applicant respectfully traverses the Examiner's rejection.

Fung teaches a power conservation system as part of a complete computer system (abstract, lines 1-3). Fung does not teach a memory specific power management scheme. Fung only teaches decreasing the frequency of refresh times of a DRAM, not varying the power level or the voltage level supplied to a memory. Also, Fung does not teach multiple voltage settings supplied specifically to a memory or to any other element of the disclosed computer system. Claims 1 and 23, on the other hand, disclose varying the power level supplied to a memory without necessarily varying the power level supplied to the rest of the system components. Therefore Fung fails to teach or suggest important elements of the Applicant's invention. Accordingly, Applicant respectfully requests withdrawal of the Examiner's rejection.

Finally, the Examiner rejected Claims 21 and 22 under 35 U.S.C. § 102(a), as being anticipated by DeLuca et al. (US Pat. No. 5,218,705). The Applicant respectfully traverses the Examiner's rejection.

As discussed above in traversing the rejection over Nakatani et al., the DeLuca reference neither discloses nor suggests providing a variable voltage to the memory element. DeLuca teaches a self-test that decreases the supplied voltage step-wise, using pre-defined voltage set points, until the system becomes inoperative. In contrast, Claim 21 of the Application recites variation of the voltage across a continuum between known operating levels without causing the memory to fail. Indeed, applying DeLuca et al.'s teaching to the invention of Claims 21 and 22 would produce an inoperable device. In fact, memory integrated circuits, and DRAMs in particular, are volatile. Thus, if the power voltage supplied

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to a memory were decreased step-wise until the memory became inoperative, all data stored in the memory would be lost. DeLuca, therefore, teaches away from the invention of Claims 21 and 22.

As a result, Applicant submits that Claims 21 and 22 are neither anticipated nor suggested by DeLuca and respectfully requests withdrawal of the Examiner's rejection.

If the Examiner's next action is other than the allowance of Claims 1-23, the Examiner is requested to call the Applicant's Attorney at (408) 453-9200.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231,

on July 24, 1997.

Alan H. MacPherson — July 24, 1997

Attorney for Applicant — Date of Signature

Respectfully submitted,

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